**module D\_latch (D, Q, En);**

**input D, En;**

**output Q;**

**assign Q = En ? D : Q;**

**endmodule**

**module test\_D\_latch;**

**// Inputs**

**reg D, En;**

**// Output**

**wire Q;**

**// Instantiate the Unit Under Test (UUT)**

**D\_latch dut (D, Q, En);**

**initial**

**begin**

**En = 1;**

**D = 1;**

**#100**

**En = 0;**

**#100**

**D = 1;**

**#100**

**En = 1;**

**#100**

**En = 1;**

**D = 0;**

**end**

**endmodule**